**In the Claims:**

Cancel claims 1-24

25. (previously added) An integrated circuit comprising:

A. a substrate;

B. operating circuits formed on the substrate, the operating circuits including an operating bus of plural leads for carrying normal operating signals;

C. a serial data input lead formed on the substrate and a serial data output lead formed on the substrate, the serial data input lead and the serial data output lead being coupled together—for carrying serial data signals on the substrate;

D. an expected data memory formed on the substrate, the expected data memory having plural expected data storage locations for storing serial data signals representing an expected data pattern and having at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead;

E. a comparator formed on the substrate, the comparator having first inputs coupled to the operating bus and having second inputs coupled to the expected data memory for comparing at least some of the normal operating signals to corresponding ones of the expected data pattern signals;

F. a command register formed on the substrate, the command register having plural command storage locations for storing serial data signals representing commands, a control input, a serial input coupled to the serial data input lead and to the command storage locations for carrying the command signals to the storage locations, and a serial output coupled to the serial data output lead;

G. a data register formed on the substrate, the data register having plural data storage locations, data inputs coupled to the data storage locations and to the first inputs of the comparator for carrying the normal operating

signals to the data storage locations, a control input, a serial input coupled to the serial data input lead and to the data storage locations for carrying the serial data signals to the data storage locations, and a serial output coupled to the serial data output lead and the data storage locations for carrying the signals in the data storage locations to the serial data output lead;

H. a mode select input lead formed on the substrate, the mode select input lead for carrying a mode select signal;

I. a serial data clock input lead formed on the substrate, the serial data clock input lead for carrying a serial data clock signal; and

J. an access port formed on the substrate, the access port including control circuitry and having a command control output coupled to the control input of the command register, a data-control output coupled to the control input of the data register, a first input coupled to the mode select input lead and a second input coupled to the serial data clock input lead, the control circuitry being operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead, and into and out of the command register, into and out of the data register, and to the expected data memory responsive to the mode select signal and the serial data clock signal.

26. (previously added) An electrical circuit comprising:

A operating circuits including an operating bus of plural leads for carrying normal operating signals;

B. a serial data input lead and a serial data output lead;

C. an expected data memory having plural expected data storage locations for storing signals representing an expected data pattern and having at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead;

D. a comparator having first inputs coupled to the operating bus and second inputs coupled to the expected data memory;

E. a command register having plural command storage locations, a control input, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead;

F. a data register having plural data storage locations, a control input, data inputs coupled to the first inputs of the comparator, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead;

G. a mode select input lead for carrying a mode select signal;

H. a serial data clock input lead for carrying a serial data clock signal;

I. an access port including control circuitry, the access port having a first input coupled to the mode select input lead, a second input coupled to the serial data clock input lead, at least one command register control output coupled to the command register control input, and at least one data register control output coupled to the data register control input; and

J. the operating circuits, the expected data memory, the comparator, the serial data input lead, the serial data

output lead, the command register, the data register, the mode select input lead, the serial data clock input lead, and the access port being permanently integrated together.

27. (previously added) An electrical circuit comprising:

A. operating circuits including an operating bus of plural leads for carrying normal operating signals;

B. a serial data input lead and a serial data output lead;

C. an expected data memory having plural expected data storage locations for storing signals representing an expected data pattern and having at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead;

D. a comparator having first inputs coupled to the operating bus and second inputs coupled to the expected data memory;

E. a data register having plural data storage locations, a control input, data inputs coupled to the first inputs of the comparator, a serial input coupled to the serial data input lead, and a serial output coupled to the serial data output lead;

F. a mode select input lead for carrying a mode select signal;

G. a serial data clock input lead for carrying a serial data clock signal;

H. an access port that includes control circuitry and that has a first input coupled to the mode select input lead, a second input coupled to the serial data clock input lead, and at least one data control output coupled to the control input of the data register; and

I. the operating circuits, the expected data memory, the comparator, the serial data input lead, the serial data output lead, the data register, the mode select input lead, the clock input lead, and the access port being permanently integrated together.

28. (previously added) The circuit of claims 25, 26 or 27 in which the control circuitry of the access port includes a state machine having inputs coupled to the mode select input lead and to the serial data clock input lead.

29. (previously added) The circuit of claim 28 including mask circuitry having plural mask storage locations for storing data signals representing a mask data pattern, and at least one input coupled to the serial data input lead and the mask storage locations for receiving the mask data pattern signals from the serial data input lead, the mask circuitry being coupled to the comparator and including circuits for masking comparison of individual normal operating signals and corresponding expected data pattern signals in response to the mask data pattern signals stored in the mask storage locations.

30. (previously added) The circuit of claim 29 in which the serial data input lead and the serial data output lead are coupled together for carrying serial data signals, and the control circuitry is operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead and into and out of the data register responsive to the mode select signal and the serial data clock signal, at least for carrying signals contained in the data storage locations of the data register to the serial data output lead.

31. (previously added) The circuit of claim 28 in which the operating bus includes a data bus of plural leads for carrying normal operating data signals and includes an address bus of plural leads for carrying normal operating address signals.

32. (previously added) The circuit of claims 25, 26, or 27 including mask circuitry having plural mask storage

locations for storing data signals representing a mask data pattern, the mask circuitry being coupled to the comparator and including circuits for masking comparison of individual normal operating signals and corresponding expected data pattern signals in response to the mask data pattern signals stored in the mask storage locations.

33. (previously added) The circuit of claim 32 in which the mask circuitry includes at least one input coupled to the serial data input lead and the mask storage locations for receiving the mask data pattern signals from the serial data input lead.

34. (previously added) The circuit of claims 25, 26, or 27 in which the serial output of the data register is coupled to the serial test data output lead through another data register and a multiplexer.

35. (previously added) The circuit of claims 26 or 27 in which the data inputs of the data register are coupled to the data storage locations of the data register and to the first inputs of the comparator for carrying the normal operating signals to the data storage locations, and the serial output of the data register is coupled to the serial data output lead and to the data storage locations for carrying the normal operating signals stored in the data storage locations to the serial data output lead.

36. (previously added) The circuit of claims 25, 26, or 27 including an operating clock lead coupled to the operating circuits for carrying an operating clock signal to the operating circuits, the operating circuits operating in normal operation in response to the operating clock signal, and at least a portion of the access port operating in a serial operation according to the serial data clock signal, and in which the serial operation of the access port is

capable of occurring during and concurrently with a portion of the normal operation of the operating circuits, so that normal operating signals from the bus can be stored in the data register and then be shifted to the serial data output lead in response to the mode select signal and the serial data clock signal while the operating circuits operate in response to the operating clock signal.

37. (previously added) The circuit of claim 25 in which the comparator has an output lead for carrying a match signal when selected ones of the normal operating signals match corresponding ones of the expected data pattern signals, the match signal requesting a serial operation during which the data register is operable to store signals from the operating bus into the data storage locations of the data register and then shift the stored signals out of the serial output of the data register and to the serial data output lead.

38. (previously added) The circuit of claims 26 or 27 in which the comparator has an output lead for carrying a match signal when selected ones of the normal operating signals match corresponding ones of the expected data pattern signals.

39. (previously added) The circuit of claim 38 in which the match signal requests a serial operation during which the data register is operable to store signals from the operating bus into the data storage locations of the data register and then shift the stored signals out of the serial output of the data register and to the serial data output lead.

40. (previously added) The circuit of claim 39 in which the expected data memory includes at least one input coupled to the serial data input lead and the plural expected data storage locations of the expected data memory for receiving

the expected data pattern signals from the serial data input lead.

41. (previously added) The circuit of claims 26, or 27 in which the operating bus includes a data bus of plural leads for carrying normal operating data signals and includes an address bus of plural leads for carrying normal operating address signals.

42. (previously added) The circuit of claim 41 in which the comparator has an output lead for carrying a match signal when at least some of the normal operating address signals on the address bus match corresponding ones of the expected data pattern signals.

43. (previously added) The circuit of claim 42 in which the comparator includes combining circuitry to combine the comparison of the expected data pattern and the normal operating address signals on the address bus with a comparison of a second expected data pattern and normal operating data signals on the data bus.

44. (previously added) The circuit of claim 43 in which the expected data memory includes at least one input coupled to the serial data input lead and the plural expected data storage locations of the expected data memory for receiving the expected data pattern signals from the serial data input lead, the circuit further including a second expected data memory having plural second expected data storage locations operable to store the second expected data pattern, the second expected data memory includes at least one input coupled to the serial data input lead and the plural second expected data storage locations for receiving the second expected data pattern signals from the serial data input lead.

45. (previously added) The circuit of claim 44 including mask circuitry having plural first mask storage locations for storing data signals representing a first mask data pattern, and at least one input coupled to the serial data input lead and the first mask storage locations for receiving the first mask data pattern signals from the serial data input lead, the mask circuitry also having second mask storage locations for storing data signals representing a second mask data pattern, and at least one input coupled to the serial data input lead and the second mask storage locations for receiving the second mask data pattern signals from the serial data input lead, the mask circuitry being coupled to the comparator and including circuits for masking comparison of individual normal operating address signals on the address bus and corresponding first expected data pattern signals in response to the first mask data pattern signals stored in the first mask storage locations and also for masking comparison of individual normal operating data signals on the data bus and corresponding second expected data pattern signals in response to the second mask data pattern signals stored in the second mask storage locations.

46. (previously added) The circuit of claim 43 in which the comparator output lead carries the match signal when there is a match both between the expected data pattern signals and at least some of the normal operating address signals on the address bus and between the second expected data pattern signals and at least some of the normal operating data signals on the data bus.

47. (previously added) The circuit of claim 25 in which the operating bus includes a data bus of plural leads for carrying normal operating data signals and includes an address bus of plural leads for carrying normal operating address signals.

48. (previously added) The circuit of claim 47 in which the comparator includes combining circuitry to combine the comparison of the expected data pattern and normal operating address signals on the address bus with a comparison of a second expected data pattern and normal operating data signals on the data bus, the comparator further including an output lead for carrying a match signal when at least one of the following conditions occur:

i) at least some of the normal operating address signals on the address bus match corresponding first expected data pattern signals, and

ii) at least some of the normal operating data signals on the data bus match corresponding second expected data pattern signals.

49. (previously added) The circuit of claim 48 in which the comparator output lead carries the match signal only when there is a match both between the expected data pattern signals and at least some of the normal operating address signals on the address bus and between the second expected data pattern signals and at least some of the normal operating data signals on the data bus.

50. (previously added) The circuit of claims 25, 26, or 27 including plural scan paths of registers connected between the serial data input lead and the serial data output lead and connected to the access port for selectively shifting and loading data signals on the scan paths in response to the mode select signal and the serial data clock signal.

51. (previously added) The circuit of claim 50 in which the expected data memory includes a register that is connected in series in a scan path and the data register is connected in series in a scan path.